Amendments to the Specification

Under the Title, Above Paragraph [0001], Replace the Section Heading as follows:

~~TECHNICAL FIELD~~ BACKGROUND OF THE INVENTION

In Between Paragraphs [0001] and [0002], Delete the Section Heading as follows:

~~PRIOR ART~~

In Between Paragraphs [0006] and [0007], Replace the Section Heading as follows:

~~DESCRIPTION OF THE INVENTION~~ SUMMARY OF THE INVENTION

In Between Paragraphs [00011] and [00012], Replace the Section Heading as follows:

~~DRAWINGS~~ BRIEF DESCRIPTION OF THE DRAWINGS

In Between Paragraphs [00014] and [00015], Replace the Section Heading as follows:

~~EMBODIMENTS~~ DETAILED DESCRIPTION

Replace Paragraph [0021] with the following Amended Paragraph:

[00021] If the electric drive 3 in accordance with the schematic circuit diagram in Figure 1 is operated in a partial load range, i.e., with a PWM timing signal < 100%, a normal operating state ensues; thus the number of edge changes 20 representing the detectable pulses is A1. This number of edge changes 20 occurring in normal operation of the electric drive 3 is stored in the micro-controller 25 (μC) and represents a reference value. If, in the evaluation circuit 37, a number of pulses, i.e., edge changes 20 at the output side 16 of the biased comparator component 14, A1* is transmitted to the input 27 of the micro-controller 25 (μC), then a comparison takes place between the number of edge changes 20 A1 occurring in normal operation and the detected number of edge changes 20 A1*. If the number A1* of edge changes 20 exceeds the number A1 of to-be-expected edge changes 20 in normal operation of the electric ~~drive 2~~drive 3 within a presettable window of time, a conclusion can be drawn that there is a defect either at the first power semiconductor component 7, at the electric drive 3 as well as in the free-wheeling circuit 6. There can also be a defect in the electrical connections. When it is established that the to-be-expected number A1 of pulses has been fallen short of by the actually detected number A1* of edge changes 20, the flow of current to the electric drive 3 is interrupted by halting the triggering via a PWM signal 29. A defect at the first power semiconductor component 7 can, e.g., be an intermittent or permanent high impedance of the first power semiconductor component that is independent of triggering.

Replace Paragraph [0024] with the following Amended Paragraph:

[00022] In the embodiment in accordance with Figure 2, an inductance designated by L is contained in the free-wheeling circuit allocated to the electric drive 3. In addition, the free-wheeling circuit 6 allocated to the electric drive 3 includes a second power semiconductor component 32. Analogous to the depiction in ~~Figure 2~~Figure 1, the voltage source 1 is integrated into the onboard network 4 of a vehicle, e.g., a motor vehicle (not shown here in more detail). The inductance as well as the capacitor 2 are connected in parallel to the voltage source 1. The triggering of the electric drive 3 is accomplished via the first power semiconductor component 7, which can be embodied, e.g., as a MOSFET or as a bipolar transistor. Its transistor base 8 (G) is acted upon by a PWM signal 31 via the triggering line 13. Analogous to the depiction in Figure 1, the first power semiconductor component 7 includes a drain gate 10 (D) as well as source gate 9 (S). The current adjusting at the first power semiconductor component 7 is indicated by the arrow designated by I and adjusts at the first power semiconductor component 7 in accordance with the PWM timing signal 31. Allocated to the first power semiconductor component 7 are the first tap 11 and the second tap 12, via which the current, the current form or voltage pulses detected from the current form are supplied to the evaluation circuit 37. The evaluation circuit 37 essentially corresponds to the evaluation circuit in the schematic circuit diagram shown in Figure 1. Also in the evaluation circuit 37 shown in Figure 2, a voltage 19 (V_{CC}) acts upon the comparator component 14. The pulses generated at the first tap 11 or at the second tap 12 arise from the switching through of the first power semiconductor component 7 in the course of triggering by the PWM timing signal 31, in which a current I adjusts via the first power semiconductor component 7, which current represents a pulse that can be evaluated or counted. Designated by I_D is the current in the drain branch 10, which flows in accordance with the PWM timing signal. The evaluatable or countable pulses arising from the flow of current through the first power semiconductor component 7 are supplied via the first tap 11 or the second tap 12 to the first comparator input 17 (-) or the second comparator input 18 (+). The current I_S detected at the second tap 12 flows via a resistor R_S, which is connected at KS to the line leading to the first comparator input 17 (-). The connecting point KS simultaneously represents a temperature detection point (Kelvin source) for the first power semiconductor component 7.